COURSE SYLLABUS

Digital Systems Test ECE 6140

Instructor: A. Chatterjee, e-mail: chat@ece.gatech.edu

Course Summary:

Digital Systems Testing is all about the science of testing the dense electronics that enables cellphones, laptops, servers, robots, self-driving cars and unmanned aerial vehicles, to name a few. The latest processors contain billions of transistors in a single integrated circuit. To make a working IC, it is necessary to ensure that not one of those transistors or the tiny wires that connect them all up together are defective. As you can well imagine this is a very difficult problem. A defective part in a self-driving car can cause accidents and create hazards. Malfunctioning hardware and software can cause havoc with servers managing financial transactions. One can come up with tons of scenarios where we need the electronics around us to be reliable. In fact, today we depend on electronics around us for our day-to-day functioning (literally). EE 6140 will focus on the core scientific aspects of delivering defect-free parts to end customers: theory and practice. The course is self-contained and will involve a project that each student will be expected to execute on an individual basis.

Course Outline

- Motivation - why test ?
- Failure mechanisms and yield models
  - parametric vs. catastrophic faults
  - impact of scaled technologies
- Theory of digital stuck-at fault testing
  - basic concepts
  - fault excitation and sensitization
  - redundant faults and coverage
  - multiple faults
- Circuit and fault simulation methods
  - digital circuits, parallel, deductive and concurrent
  - analog circuits
- Test generation algorithms and test methods
  - digital, stuck-at and delay faults
  - delay fault testing
  - analog/RF
- Memory Testing
  - March tests
  - Testing for pattern sensitive failures
- Current based testing methods
- Design for testability techniques
  - scan
  - JTAG, boundary scan
  - test response compression
- Built-in self-test
  - LFSR theory
  - built-in test architectures

- Self-calibration techniques
  - post manufacture circuit tuning for repair/yield-enhancement
- New topics in test
  - analog/mixed-signal circuit testing
  - testing of deeply scaled CMOS devices
  - test methods for neuromorphic networks

Grading:
Test 1: 20%
Test 2: 20%
Final: 30%
HW: 5%
Project: 25%

Project: The project will involve writing a fault simulator and test vector generator for digital combinational circuits in a language of your choice. At the end of the semester, every student will be required to demonstrate both components of the project on "surprise" test cases that will be used to evaluate the correctness of the implemented algorithms.

The instructor, Prof. Chatterjee can be reached via e-mail: chat@ece.gatech.edu Please use the e-mail heading "ECE 6140" when communicating with the instructor throughout the semester.

Textbook: Digital Systems Testing & Testable Design by Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman